GaAs Ultra-High-Frequency Dividers with Advanced SAINT FET's

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Abstract—**The circuit design, fabrication, and performance of ultra-high-frequency dividers with buffer FET logic (BFL) circuits are described. Using air-bridge technology and a new, self-aligned-gate, GaAs FET process, called advanced SAINT, which avoids excess gate metal overlap on the dielectric film, 10.6-GHz operation at 258 mW is achieved. This performance is made possible by a reduction of gate and interconnection parasitic capacitance. Furthermore, the possibility of operation above 20 GHz for GaAs MESFET frequency dividers is predicted on the basis of circuit optimization and FET improvements including parasitic capacitance reduction and transconductance enhancement.**

I. Introduction

HIGH-SPEED GaAs LSI's, such as the 16-kbit SRAM [1] and 2-Gbit/s time switch [2] have been developed with SAINT FET's [3]. GaAs MSI's and SSI's have great potential in satellite and microwave communications systems because of their ultra-high-frequency operation, low power consumption, and radiation hardness. A frequency divider operating at a higher frequency and with lower power is required to simplify the phase-locked loop for the local oscillator circuits in such systems.

Various circuit configurations for GaAs ultra-high-frequency dividers, such as buffered FET Logic (BFL) [4], source-coupled FET logic (SCFL) [5], and direct-coupled FET logic (DCFL) [6], have previously been investigated. BFL circuits have the advantages of high-speed operation and simple configuration, consisting of only MESFET's, because diodes are constructed by the same MESFET's with connection between the source and drain. In addition, BFL circuits have high driving capability.

In this paper, circuit design, fabrication, and performance improvements of a GaAs BFL ultra-high-frequency divider are described. As a result of circuit optimization, a binary frequency divider using BFL circuits with a source follower proved to operate faster than one having only level shift diodes. Therefore, the former circuit configuration was adopted for circuit fabrication. For parasitic capacitance reduction, a new FET fabrication process, called advanced SAINT [7], has been developed. It utilizes a self-aligned gate formation technology so as to avoid the excess gate metal overlap upon dielectric film that causes parasitic capacitance in conventional SAINT FET's [3]. The second-level interconnection lines have been constructed by air-bridge technology, minimizing parasitic capacitance between lines.

Using these technologies, BFL M/S binary frequency dividers were fabricated with 0.5-μm-gate FET's and operated at 10.6 GHz with 258-mW power dissipation. In addition, the potential operation of GaAs MESFET static frequency dividers above 20 GHz is also described.

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II. Circuit Design

Two types of BFL circuits consisting of different output circuit configurations (A and B) [4] were studied. These circuit configurations are shown in Fig. 1. The type A circuit uses a source follower in the level shift position to ensure a large driving capability. The type B circuit uses only diodes in the level shift position. These circuits were applied to a two-level series gating master–slave flip-flop circuit considered to be capable of the highest frequency operation. High-frequency operation of the binary frequency dividers with BFL circuits A and B were simulated under standard supply voltages of $V_{DD} = 3$ V and $V_{SS} = -2$ V by improved SPICE II, using FET and diode models including parasitic capacitance [8]. FET gate parasitic capacitance C_P was simply defined as parallel capacitance to gate–source capacitance C_{gs} or gate–drain capacitance C_{gd}. The FET parameters used in the simulation were a gate length L_g of 0.5 μm, a threshold voltage V_{th} of -1 V, a transconductance g_m of 200 mS/mm, and a gate parasitic capacitance C_P of 3 fF/40-μm gate width. Interconnection capacitance was not included.

Simulation results indicating the dependence of maximum operation frequency $f_{c\max}$ on driver FET gate width W_g are shown in Fig. 1. It can be seen that the frequency divider constructed with type A BFL circuits, permitting large driving capability, allows an approximately 1-GHz improvement in operation frequency compared to type B BFL circuits, and that the maximum operation frequency shows a saturation tendency at $W_g = 30$–40 μm. The power dissipation of type A circuits is slightly higher than that of type B circuits. As shown in Fig. 2, type A BFL circuits for binary frequency dividers were used in our experiments, along with a W_g of 40 μm. The following calculations and experiments were carried out using the type A circuit.

Fig. 3 shows circuit simulation results of the dependence of the maximum operation frequency on FET gate parasitic capacitance C_p using standard supply voltages, with and without interconnection capacitance in the case of

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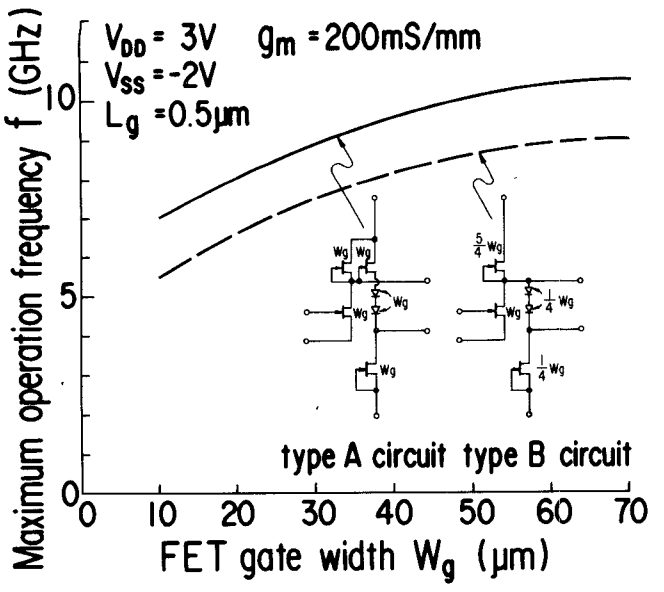


Fig. 1. Maximum operation frequency dependence of two types of frequency dividers on driver FET gate width. Type A BFL circuit uses a source follower in the level shift position to ensure a large driving capability. Type B BFL circuit uses only diodes in the level shift position.

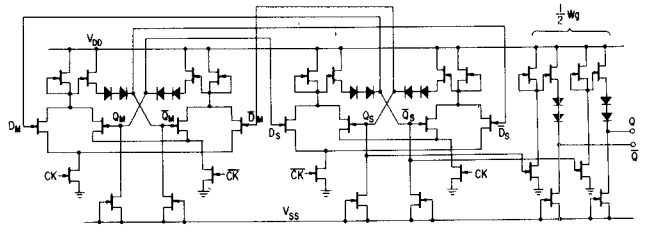


Fig. 2. Schematic diagram of a binary frequency divider with output buffers using type A BFL circuits. FET gate width is 40 μm except FET's with 20-μm gate width denoted as $\frac{1}{2}W_g$.

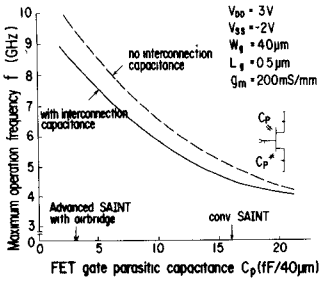


Fig. 3. Simulated maximum operation frequency dependence on FET gate parasitic capacitance with or without interconnection capacitance. C_p is defined as parallel capacitance to gate–source capacitance C_{gs} or gate–drain capacitance C_{gd}.

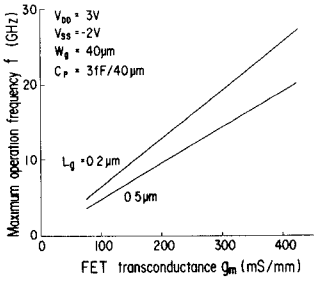


Fig. 4. Simulated maximum operation frequency dependence on FET transconductance with reduced parasitic capacitance.

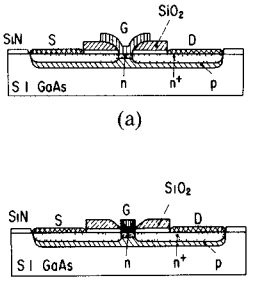


Fig. 5. Cross-sectional views of (a) a conventional FET and (b) an advanced SAINT FET.

type A circuits, as shown in Fig. 2. Other FET parameters were the same as those used in Fig. 1 except for a gate width of 40 μm. In the conventional SAINT FET with the excess gate overlap, C_p was estimated to be 16 fF/40-μm gate width as measured from the frequency divider. It is expected that the reduction of gate and interconnection parasitic capacitance will be remarkably effective for high-frequency operation.

Maximum operation frequency dependence on FET transconductance was simulated with reduced FET and interconnection parasitic capacitance under standard supply voltages using the type A circuits shown in Fig. 2. Calculations of 0.2-μm-gate FET's were carried out in addition to the FET parameters used in Fig. 1. As shown in Fig. 4, a maximum operation frequency higher than 20 GHz is predicted at a gate length of 0.2 μm and a transconductance of 400 mS/mm, attainable by gate-length shortening and active layer thinning.

III. Fabrication Process

Schematic cross-sectional views of conventional and advanced SAINT FET's are shown in Fig. 5. In the advanced SAINT FET structure, there is no gate metal overlapping, the cause of parasitic capacitance in the conventional SAINT FET.

The advanced SAINT fabrication process [7] is almost the same as the conventional [3] except for gate formation. The gate electrode formation process involves the following steps, as shown in Fig. 6: 1) Mo and Au are deposited onto the whole surface by sputtering (Fig. 6(a)); 2) the Au surface is planarized by ion beam milling with a large beam incident angle (Fig. 6(b)); and 3) using this Au pattern as the etching mask, Mo film is selectively etched by RIE (Fig. 6(c)). Consequently, the gate electrode is embedded in a self-aligned manner only in the gate contact region. After gate formation, source and drain ohmic electrodes were formed by AuGe/Ni deposition and sintering.

With self-aligned gate electrode formation, FET's having a gate length of only 0.2 μm were successfully fabricated without excess gate metal overlap on the dielectric film.

In addition to FET structural improvements, second-level interconnection lines were constructed using "air-

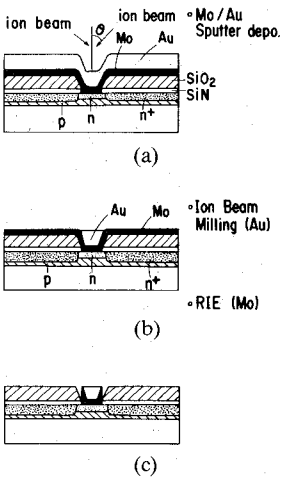


Fig. 6. Gate formation steps in the advanced SAINT FET fabrication process.

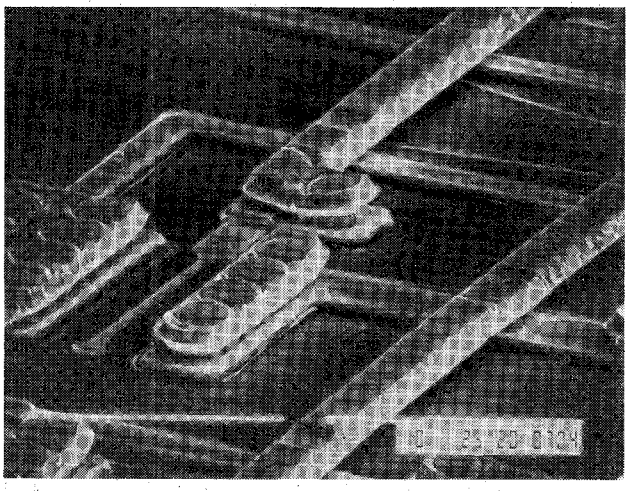


Fig. 7. An SEM photograph of air-bridge lines and an FET.

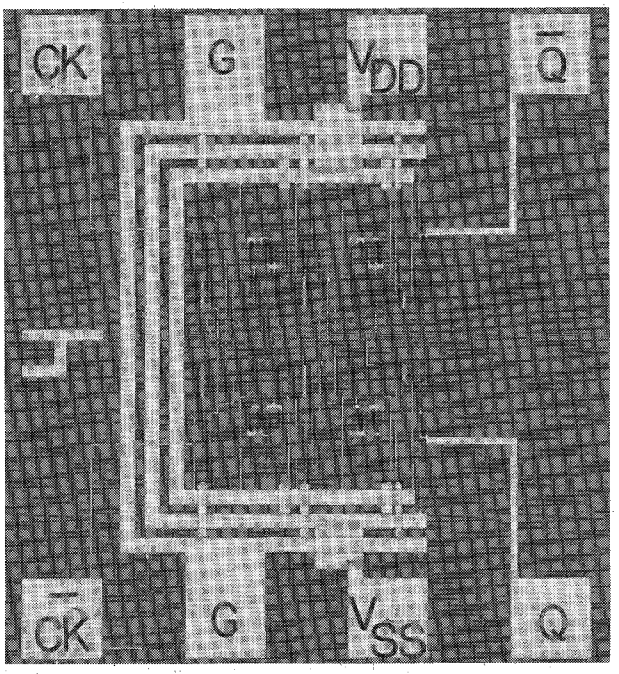
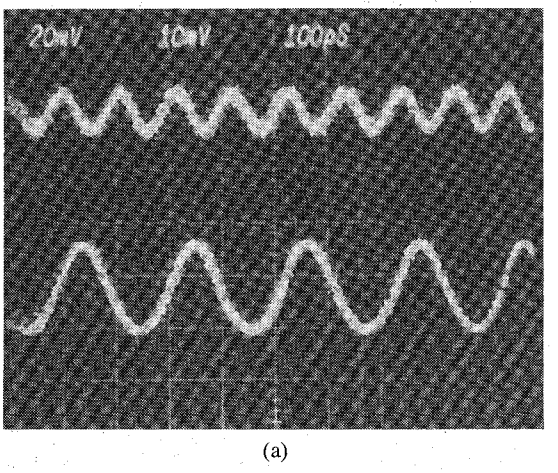
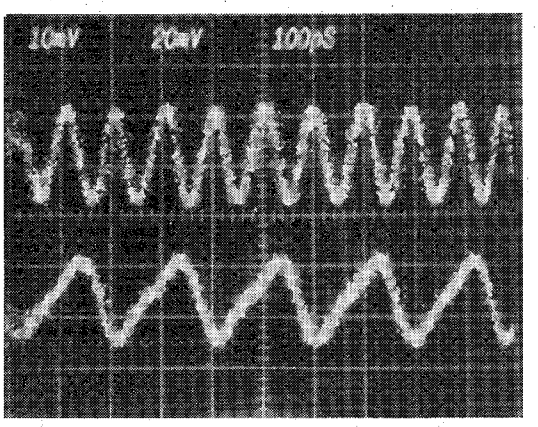


Fig. 8. A microphotograph of a BFL M/S binary frequency divider. Chip size is 0.87×1 mm^2.



(a)



(b)

Fig. 9. Operation waveforms of a BFL M/S binary frequency divider using the following two kinds of supply voltages: (a) V_{DD} 3 V, V_{SS} −2 V; power dissipation—200 mW, clock input—9.6 GHz, 1.2 V (peak–peak), output: 4.8 GHz, and 180 mV (peak–peak); (b) V_{DD} 3.4 V, V_{SS} −3.1 V, power dissipation: 258 mW, clock input: 10.6 GHz, 1.1 V(peak–peak), output: 5.3 GHz, and 24 mV(peak–peak).

bridge" technology. Though two-level interconnection technology, using SiN or SiO_2 as the interlayer is popular, the high dielectric constant of the interlayer increases between line capacitance and degrades IC high-frequency performance. In order to minimize between line capacitance, it is necessary to construct the second-level interconnection line by air-bridge technology, which yields an ideal interlayer dielectric constant. An SEM photograph of the air-bridge lines and an FET is shown in Fig. 7.

Binary frequency dividers were fabricated with advanced SAINT and air-bridge technology. The gate length and the threshold voltage of FET's, were 0.5 μm and −1 V, respectively, where the transconductance was 200 mS/mm. Although the fabrication of an 0.2-μm-gate-length FET could be achieved by using advanced SAINT technology, the yield was insufficient for frequency divider IC's. To date, only the use of 0.5-μm-gate-length FET's for IC fabrication has been achieved. Ultra-high-frequency divider IC's with 0.2-μm-gate-length advanced SAINT FET's are now under fabrication. The circuit geometry was optimized and made compact by symmetric circuit arrangement and short interconnections. A photograph of

a fabricated circuit is shown in Fig. 8. Chip size is 0.87×1 mm^2.

IV. Measurement Results

High-frequency measurements were carried out with a high-frequency probe card at room temperature. Under standard biases of $V_{DD} = 3$ V and $V_{SS} = -2$ V, the maximum operation frequency was 9.6 GHz, as shown in Fig. 9(a), which corresponds to the simulation results (Figs. 3 and 4). The difference in gate parasitic capacitance C_p between the advanced SAINT and the conventional can be estimated to be 13 fF/40-μm gate width, comparing measured maximum operation frequencies, 9.6 GHz and 6.8 GHz, respectively, in Fig. 3. This parasitic capacitance reduction is thought to be due to the removal of excess gate metal overlaps by self-aligned gate electrode formation.

Under optimized supply voltages of $V_{DD} = 3.4$ V at 48 mA and $V_{SS} = -3.1$ V at 30 mA, a maximum toggle frequency of 10.6 GHz was obtained at 258-mW power dissipation, as shown in Fig. 9(b) [9]. The internal logic swing was 180 mV_{p-p} in the dividing operation shown in Fig. 9(b), although the output swing was as small as 24 mV_{p-p} because a 50-Ω load was used at the point of measurement. A lower power dissipation will occur in the case of a threshold voltage higher than -1 V. The maximum toggle frequency is 4 GHz higher than that of a frequency divider, 6.8 GHz, the latter consisting of identically sized FET's fabricated by conventional SAINT and conventional two-level interconnection technology with a SiN interlayer dielectric film [10].

V. Conclusions

Aiming at ultra-high-frequency operation, a frequency divider circuit design, the reduction of FET, and interconnection parasitic capacitance were studied. Advanced SAINT, having gate electrodes without excess overlap upon dielectric film, and applied air-bridge technology successfully reduced parasitic capacitance around the gate and between interconnection lines. Using these technologies, at room temperature, a BFL binary frequency divider with 0.5-μm-gate FET's achieved 10.6-GHz operation at 258 mW.

Circuit simulation with empirical FET parameters predicts the possibility of high-frequency operation above 20 GHz for GaAs static frequency dividers using advanced SAINT FET's with an 0.2-μm gate length and air-bridge interconnections. This divider IC using GaAs BFL circuits can be effectively applied to satellite and microwave communications.

Acknowledgment

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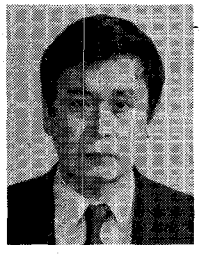

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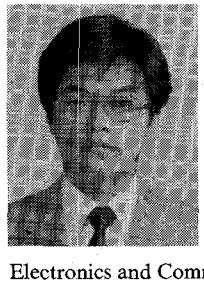

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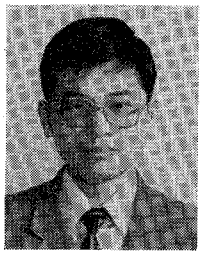

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